Supplementary Information for Towards High-Resolution and High-Brightness Uniformity Near-Eye Display: Heterogeneous Integration of GaN-based Micro-LED on a Custom Si CMOS Platform

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The PDF file includes:
Fig. S1 to Fig. S3

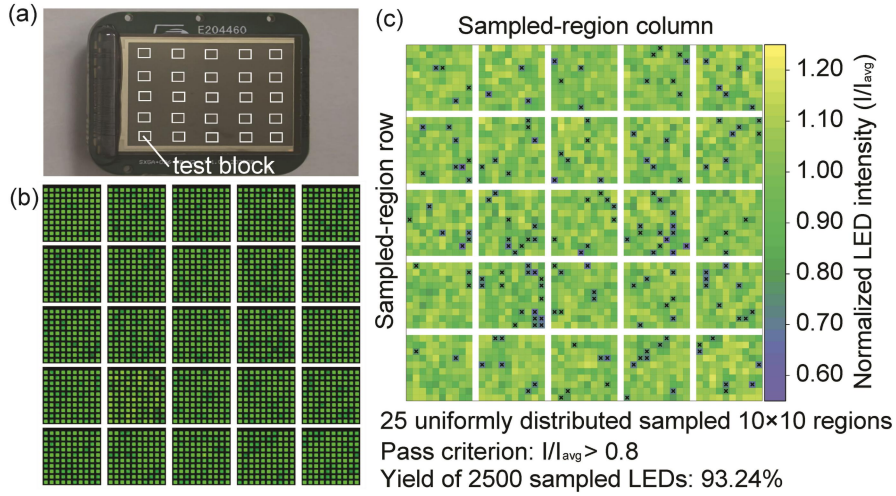

Fig. S1 Pixel yield measurement. (a) The 25 test blocks uniformly distributed on the micro-LED screen. (b) Luminescence of 100 pixels in each test block. (c) Luminous intensity distribution of 2500 pixels.

25 blocks were uniformly selected on the display screen, with each block covering 100 pixels, as illustrated in Fig. S1(a). The luminous intensity of each pixel in these blocks shown in Fig. S1(b) was measured using a micro screen optical and color test system (Model C151-3.5X). The average luminous intensity of the 100 pixels in each block was recorded as I(i). The overall average luminous intensity I_{avg} of all micro-LED pixels was obtained by averaging the data from 2500 pixels across all test blocks. A pixel was defined as a defective pixel when $I(i)<0.8 \cdot I_{avg}$. Fig. S1(c) shows the distribution of pixel luminous intensity derived from I(i) and I_{avg} , in which the luminous intensity has been normalized. The average intensity I_{avg} is normalized to 1, so pixels with $I(i)<0.8$ are identified as defective pixels. A total of 169 pixels exhibited luminous intensity lower than 80% of the average intensity.

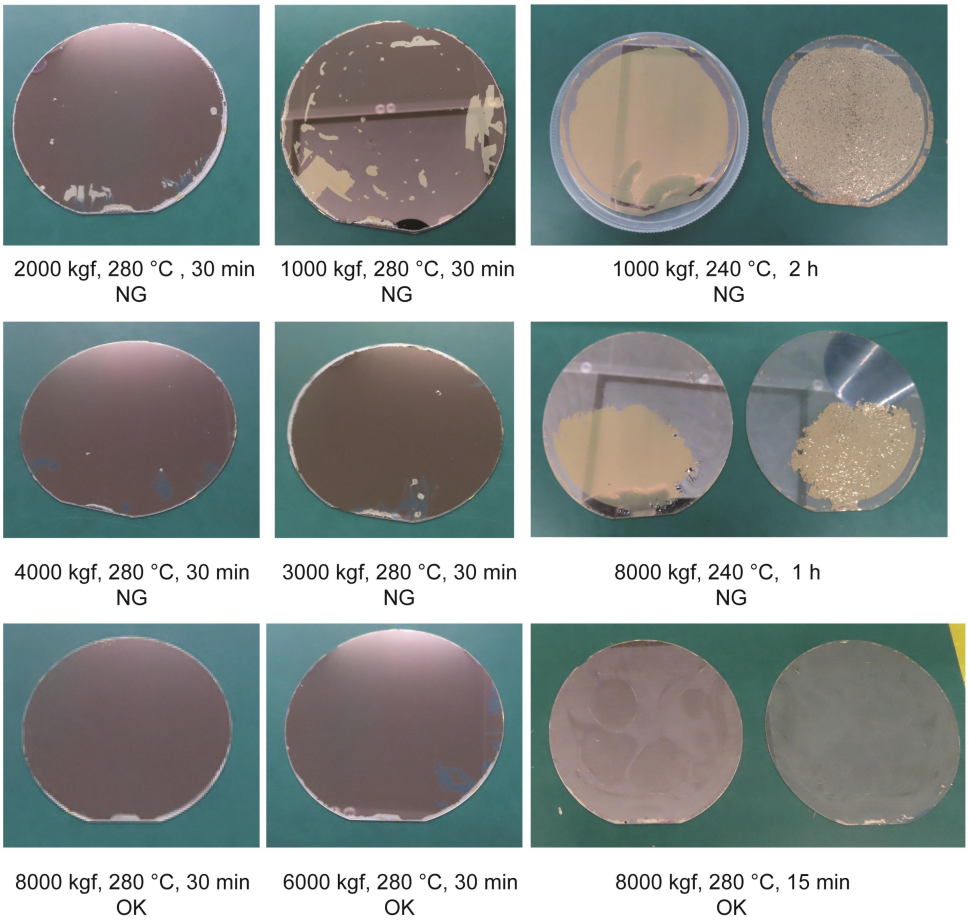

Fig. S2 Wafer bonding test based on 4-inch Si wafers.

Wafer bonding process optimization was carried out on a 4-inch Si wafer, with bonding temperature and pressure as the two key variables. Two representative bonding temperatures were adopted: 240 ℃ and 280 ℃, while the bonding pressure was varied from 1000 kgf to 8000 kgf. Following wafer bonding, laser lift-off (LLO) was performed to remove the sapphire substrate, and the integrity of the transferred LED epitaxial films was evaluated by tape peeling test. A moderate temperature near the eutectic point forms a uniform liquid interlayer, which fully wets the interface, fills microscale gaps, and reduces voids. It also softens the bonding layer to relieve stress concentration through plastic flow and deformation. Too low a temperature produces insufficient liquid phase, leading to poor bonding and residual stress. Too high a temperature aggravates thermal expansion mismatch, increases wafer warpage and interfacial tensile stress, and causes interfacial cracks and defects. An appropriate pressure compensates for contact non-uniformity from wafer warpage, removes

interfacial voids, and discharges trapped gas. It also generates compressive stress to offset thermally induced tensile stress and lower cracking risk. Insufficient pressure results in weak contact and numerous unbonded regions, while excessive pressure squeezes out molten solder (risking short circuits) and introduces extra mechanical stress that worsens warpage and interfacial fracture.

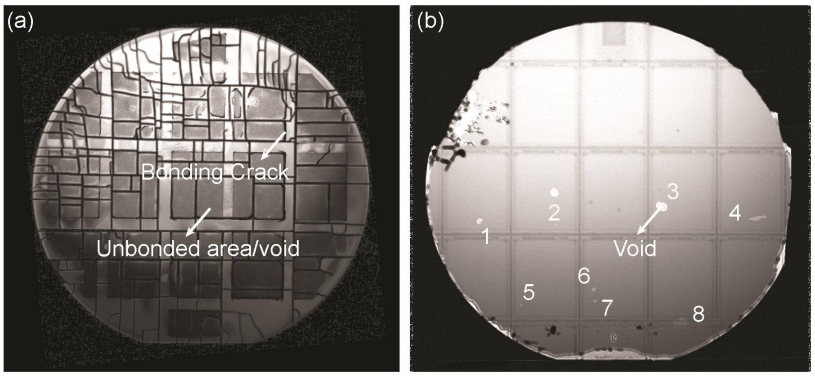

Fig. S3 SAM image of the bonded LED epi-wafer and CMOS wafer. (a) Shows severe bonding voids within the bonding layer, as well as obvious cracks on the CMOS substrate and at the bonding interface before process optimization; (b) No bonding cracks were observed and the void density was drastically reduced after process optimization.

The 4-inch CMOS substrate contains 11 intact 0.99-inch driving circuit units with a total area of approximate 35 cm^2, across which only eight voids were observed, corresponding to a void density of approximately 0.23 cm^{-2}. Furthermore, wafer warpage also plays a critical role in determining the bonding yield. In general, Si wafers exhibit significantly lower warpage than sapphire-based LED wafers. We therefore adopted a strategy of selecting sapphire LED wafers with bow values below 60 μm, which effectively ensures a high bonding yield based on our practical experience.