Supplementary Information for Nanoscale characterisation of stress in Si nanowires for semiconductor qubit fabrication

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S1 Z-coordinate Raman linescans

Figure S1 shows the full range of Raman measurements as a function of the z-coordinate. The z = 0 coordinate marks the position of the NW. As detailed in the main text, when the laser beam directly focuses on the NW, the derived temperature could be relatively high (up to 1000 K). Also, the naive mathematical calculation of the stress values reaches up to 7 GPa. In this temperature range, the assumptions made in the model are no longer valid and stress and temperature cannot be extracted with our relatively simple mathematical treatment. Furthermore, as the desired stress value is that at room temperature, such high temperature regimes are not required, or even desirable, for a correct assessment of the NW stress.

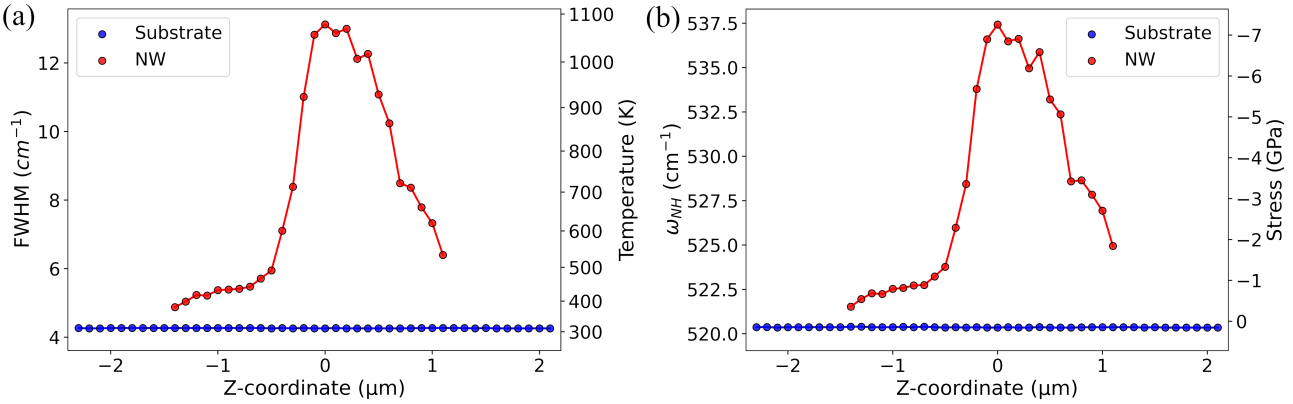


Figure S1: (a) FWHM of the NW (red) and substrate (blue) Raman signals, together with the corresponding temperature (right y-axis), as a function of the z-coordinate along the linescan. Full range. (b) Raman shift of the NW (red) and substrate (blue) Raman signals, together with the corresponding stress (right y-axis), as a function of the z-coordinate along the linescan. Full range.

S2 Sample fabrication

The devices were fabricated on a 4-inch silicon-on-insulator (SOI) wafer using a multi-step lithographic process. The wafer contains over 5000 individually addressable SiNWs, each connected to source and drain electrodes and routed to dedicated electrical contact pads. This high-density layout enables large-scale statistical analysis and parallel electrical characterization. To define free-standing Si NWs, the bulk silicon and the buried oxide (BOX) layer were selectively removed from the backside of the wafer. This was achieved by aligning a backside lithography step to front-side alignment marks, followed by etching through the silicon substrate by KOH and the BOX layer by diluted HF. The resulting structure isolates the NWs and enables optical access and mechanical decoupling. Figure S2 presents representative images of the fabrication of the structures: (a) Dark-field optical microscopy image showing a NW, its electrical tracks, and alignment marks. (b) Atomic force microscopy (AFM) image of a NW with two triangular tapering connections to the metal tracks. (c) Confocal microscopy image showing a NW resting on the SiO_2 membrane (BOX layer) before releasing the BOX layer, highlighting the etched backside cavity reaching the BOX layer.

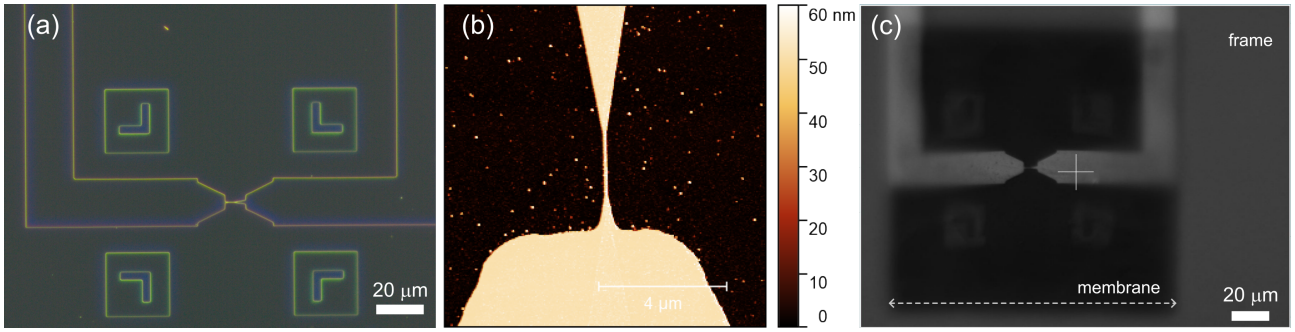


Figure S2: Images of SiNWs at different stages of the fabrication process: (a) and (b) show the structures before membrane definition by KOH, while (c) illustrates the device after membrane fabrication and just before its release from the SiO_2 membrane. (a) Dark-field optical image of a NW device showing electrical tracks and alignment marks. (b) AFM image of the NW with triangular tapering connections to the tracks. (c) Confocal image of the NW on top of the SiO_2 membrane, where bulk silicon has been etched back to the BOX layer. The membrane appears darker due to reduced light backscattering, as illumination comes from the front side and less light is reflected from the etched cavity compared to the surrounding bulk silicon.